CLAIMS

1. (Currently amended) A semiconductor device, comprising:

a transmitter capable of encoding first and second input signals as a plural-bit symbol signal responsive to first and second clocks, respectively, the first clock being out of phase from the second clock; and

a receiver capable of generating first and second output signals by decoding the symbol signal responsive to third and fourth clocks, respectively, and capable of generating first and second even and odd data.

2. (Original) The semiconductor device of claim 1 where the plural-bit symbol signal is at least two bit data.

3. (Original) The semiconductor device of claim 2 where the at least two bit data is a three level data.

4. (Original) The semiconductor device of claim 3 where the three level data includes a first, second, and third levels.

5. (Original) The semiconductor device of claim 2 where the at least two bit data is a four level data.

6. (Original) The semiconductor device of claim 5 where the four level data includes a first, second, third, and fourth levels.

7. (Original) The semiconductor device of claim 1 where the second clock is 90 degrees out of phase from the first clock.

8. (Original) The semiconductor device of claim 1 where the fourth clock is 90 degrees out of phase from the third clock.

9. (Original) The semiconductor device of claim 1 where the symbol signal comprises a plurality of symbols.

10. (Canceled)

11. (Original) The semiconductor device of claim 1 where the transmitter comprises:

a first transmitting circuit capable of generating a first transmitting signal by manipulating the first input signal responsive to the first clock;

a second transmitting circuit capable of generating a second transmitting signal by manipulating the second input signal responsive to the second clock; and

a superposition node capable of generating the symbol signal by super-positioning the first and second transmitting signals.

12. (Original) The semiconductor device of claim 1 where the receiver comprises:

a first receiving circuit capable of generating the first output signal by manipulating the symbol signal responsive to the third and a fifth clocks, the fifth clock being out of phase from the third clock; and

a second receiving circuit capable of generating the second output signal by manipulating the symbol signal responsive to the fourth and a sixth clocks, the sixth clock being out of phase from the fourth clock.

13. (Original) The semiconductor device of claim 12

where the fifth clock is 180 degrees out of phase from the third clock; and

where the sixth clock is 180 degrees out of phase from the fourth clock.

14. (Currently amended) The semiconductor device of claim 12

where the first receiving circuit is capable of generating the first even and odd data responsive to the third and fifth clocks, respectively; and

where the second receiving circuit is capable of generating the second even and odd data responsive to the fourth and sixth clocks, respectively.

15. (Original) The semiconductor device of claim 14 where the first receiving circuit comprises:

a first detector capable of generating the first even and odd data according to a medium reference voltage;

a second detector capable of generating first select signal by detecting midlevel data according to high and low reference voltages; and

a multiplexer capable of selecting between the first even and the second odd data and the first odd and the second even data responsive to the select signal.

16. (Original) The semiconductor device of claim 14 where the second receiving circuit comprises:

a first detector capable of generating the second even and odd data according to a medium reference voltage;

a second detector capable of generating a select signal by detecting midlevel data according to high and low reference voltages; and

a multiplexer capable of selecting between the first and second even data and the first and second odd data responsive to the select signal.

17. (Currently amended) A device, comprising:

transmitting means capable of encoding input data as plural-bit symbol data responsive to at least two transmitting clocks out of phase from each other; and

receiving means capable of generating output data and first and second even and odd data by decoding the symbol data responsive to at least two receiving clocks.

18. (Original) The device of claim 17 where the plural-bit symbol data is at least two bit data.

19. (Original) The device of claim 17 where the at least two transmitting clocks are 90 degrees out of phase from each other.

20. (Original) The device of claim 17 where the at least two receiving clocks are 90 degrees out of phase from each other.

21. (Canceled)

22. (Original) The device of claim 17 where the transmitting means comprises:

first transmitting circuit means capable of generating a first transmitting signal by manipulating the input data responsive to one of the at least two transmitting clocks;

second transmitting circuit means capable of generating a second transmitting signal by manipulating the input data responsive to another of the at least two transmitting clocks; and

superposition means capable of generating the symbol data by super-positioning the first and second transmitting signals.

23. (Original) The device of claim 17 where the receiving means comprises:

first receiving circuit means capable of generating first output data by manipulating the symbol data responsive to one of the at least two receiving clocks; and

second receiving circuit means capable of generating second output data by manipulating the symbol data responsive to another of the at least two receiving clocks.

24. (Currently amended) The device of claim 23 where the first receiving circuit means comprises:

first detecting means capable of generating first pre even and pre odd data according to a medium reference voltage;

second detecting means capable of generating the first odd and even select signals by detecting midlevel data according to high and low reference voltages; and

first multiplexing means capable of selecting between the first pre even and pre odd data and second even and odd data responsive to the first odd and even select signals, respectively.

25. (Original) The device of claim 24, further comprising:

first generating means generating first even and odd data responsive to one of the receiving clocks.

26. (Original) The device of claim 25 where the second receiving circuit means comprises:

third detecting means capable of generating second pre even and pre odd data according to the medium reference voltage;

fourth detecting means capable of generating second odd and even select signals by detecting midlevel data according to the high and low reference voltages; and

second multiplexing means capable of selecting between the second pre even and pre odd data and first even and odd data responsive to the second odd and even select signals, respectively.

27. (Original) The device of claim 26, further comprising:

second generating means generating second even and odd data responsive to the other of the receiving clocks.

28. (Original) A receiver, comprising:

a first receiving circuit capable of generating first output data and first even and odd data by manipulating symbol data responsive to a first and second clocks, the first output data being single bit data, the symbol data being plural-bit data;

a second receiving circuit capable of generating second output data and second even and odd data by manipulating the symbol data responsive to a third and fourth clocks, the second output data being single bit data;

where the second clock is out of phase from the first clock and the fourth clock is out of phase from the third clock.

29. (Original) The receiver of claim 28

where the first receiver is capable of receiving the second even and odd data; and

where the second receiver is capable of receiving the first even and odd data.

30. (Original) The receiver of claim 28 where the first receiving circuit comprises:

a first detector capable of generating first pre odd and pre even data responsive to a medium reference voltage;

a second detector capable of generating first odd and even select signals by detecting midlevel data responsive to high and low reference voltages; and

a multiplexer capable of selecting between the first pre even data and the second odd data responsive to the first even select signal and between the first pre odd data and the second even data responsive to the first odd select signal.

31. (Original) The receiver of claim 30

where the second detector is capable of operating responsive to a plurality of first and a plurality of second phase clocks derived from the first and second clocks, respectively, the first phase clocks having a different duty cycle than the first clocks and the second phase clocks having a different duty cycle than the second clocks.

32. (Original) The receiver of claim 30 where the second receiving circuit comprises:

a third detector capable of generating second pre odd and pre even data responsive to the medium reference voltage;

a fourth detector capable of generating second odd and even select signals by detecting midlevel data responsive to the high and low reference voltages; and

a multiplexer capable of selecting between the second pre even data and the first even data responsive to the second even select signal and between the second pre odd data and the first odd data responsive to the second odd select signal.

33. (Original) The receiver of claim 32

where the fourth detector is capable of operating responsive to a plurality of third and a plurality of fourth phase clocks derived from the third and fourth clocks, respectively, the third phase clocks having a different duty cycle than the third clocks and the fourth phase clocks having a different duty cycle than the fourth clocks.

34. (Currently amended) A transmitter, comprising:

a first driver capable of generating first transmit data responsive to a first transmitting clock; ~~and~~

a second driver capable of generating second transmit data responsive to a second transmitting clock, ~~; and~~ the first transmitting clock ~~is~~ being out of phase relative to the second transmitting clock; and

a superposition node adapted to superposition the first and second transmit data to generate multi-bit symbol data.

35. (Original) The transmitter of claim 34 where the symbol data represents at least two bit data.

36. (Original) The transmitter of claim 34 where the second transmitting clock is 90 degree out of phase of the first transmitting clock.

37. (Original) The transmitter of claim 34 where the second transmitting clock is half bit time out of phase of the first transmitting clock.